V_{SM}	=	6500 V
I_{TAVM}	=	1580 A
I_{TRMS}	=	2480 A
I_{TSM}	=	29700 A
V_{T0}	=	1.2 V
r_T	=	0.458 mΩ

Bi-Directional Control Thyristor

5STB 18U6500

Doc. No. 5SYA1037-02 Apr. 02

- **Two thyristors integrated into one wafer**
- **Patented free-floating silicon technology**
- **Designed for traction, energy and industrial applications**
- **Optimum power handling capability**
- **Interdigitated amplifying gate.**

The electrical and thermal data are valid for one thyristor half of the device.

Blocking Maximum rated values

Symbol	Conditions	5STB 18U6500	5STB 18U6200	5STB 18U5800
V_{SM}	f = 5 Hz, t_p = 10ms	6500 V	6200 V	5800 V
V_{RM}	f = 50 Hz, t_p = 10ms	5600 V	5300 V	4900 V
I_{RM}	V_{RM}, T_j = 110°C	≤ 600 mA		
dV/dt_{crit}	Exp. to 0.67 x V_{DRM}, T_j = 110°C	2000 V/µs		

Mechanical data

Parameter	Symbol	Conditions	min	typ.	max	Unit
Mounting force	F_M		120	135	160	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2
Weight	m			3.6		kg
Surface creepage distance	D_S		53			mm
Air strike distance	D_a		22			mm

On-state

Parameter	Symbol	Conditions	min	typ.	max	Unit
Max. average on-state current	I_{TAVM}	Half sine wave, T_c = 70°C	1580			A
Max. RMS on-state current	I_{TRMS}		2480			A
Max. peak non-repetitive surge current	I_{TSM}	tp = 10 ms, Tj = 110°C, V = V_R=0 V	29700			A
Limiting load integral	I^2t		4400			kA^2s
Max. peak non-repetitive surge current	I_{TSM}	tp = 8.3 ms, Tj = 110°C, V = V_R=0 V	31800			A
Limiting load integral	I^2t		4190			kA^2s
On-state voltage	V_T	I_T = 1600 A, T_j= 110°C			1.93	V
Threshold voltage	V_{T0}	I_T = 1000 A - 3000 A, T_j= 110°C			1.2	V
Slope resistance	r_T	Tj = 110°C			0.458	mΩ
Holding current	I_H	T_j = 25°C			125	mA
		T_j = 110°C			75	mA

Switching

Parameter	Symbol	Conditions		min	typ.	max	Unit
Critical rate of rise of on-state current	di/dt_{crit}	T_j = 110°C, I_{TRM} = 2000 A, $V_D \le 0.67 \cdot V_{RM}$, I_{FG} = 2 A, t_r = 0.5 µs	Cont. f = 50 Hz			250	A/µs
Critical rate of rise of on-state current	di/dt_{crit}		Cont. f = 1Hz			1000	A/µs
Delay time	t_d	$V_D = 0.4 \cdot V_{RM}$, I_{FG} = 2 A, t_r = 0.5 µs				3	µs
Turn-off time	t_q	T_j = 110°C, I_{TRM} = 2000 A, V_R = 200 V, di_T/dt = -1.5 A/µs, $V_D \le 0.67 \cdot V_{RM}$, dv_D/dt = 20V/µs,				800	µs
Recovery charge	Q_{rr}	T_j = 110°C, I_{TRM} = 2000 A, V_R = 200 V, di_T/dt = -1.5 A/µs		2100		3200	µAs

Triggering

Parameter	Symbol	Conditions	min	typ.	max	Unit
Gate trigger voltage	V_{GT}	T_j = 25°C			2.6	V
Gate trigger current	I_{GT}	T_j = 25°C			400	mA
Gate non-trigger voltage	V_{GD}	V_D = 0.4 x V_{RM}, T_{vjmax} = 110°C	0.3			V
Gate non-trigger current	I_{GD}	V_D = 0.4 x V_{RM}	10			mA
Peak forward gate voltage	V_{FGM}				12	V
Max. rated peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Max. rated gate power loss	P_G	For DC gate current			3	W
Max. rated peak forward gate power	P_{GM}			see Fig. 9		

Thermal

Parameter	Symbol	Conditions	min	typ.	max	Unit
Operating junction temperature range	T_j				110	°C
Storage temperature range	T_{stg}		-40		140	°C
Thermal resistance junction to case	R_{thJC}	Double side cooled			8	K/kW
		Anode side cooled			16	K/kW
		Cathode side cooled			16	K/kW
Thermal resistance case to heatsink	R_{thCH}	Double side cooled			1.6	K/kW
		Single side cooled			3.2	K/kW

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^{n} R_i (1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i(K/kW)	5.11	1.63	0.85	0.45
τ_i(s)	0.9531	0.1541	0.0211	0.0068

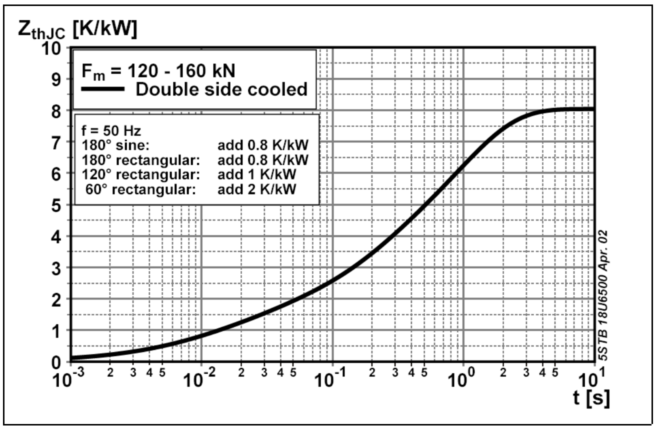

Fig. 1 Transient thermal impedance junction to case

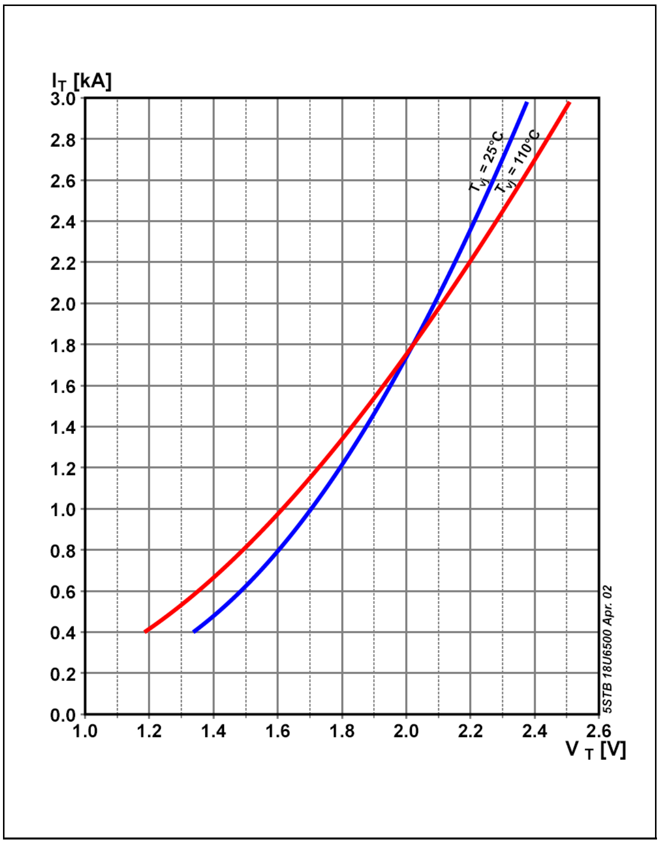

Fig. 2 Isothermal on-state characteristics

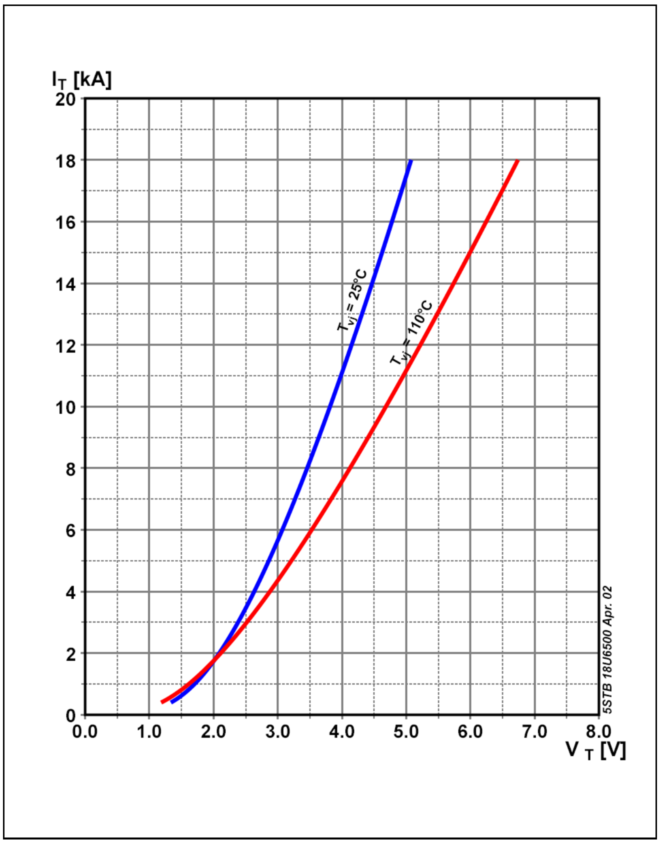

Fig. 3 Isothermal on-state characteristics

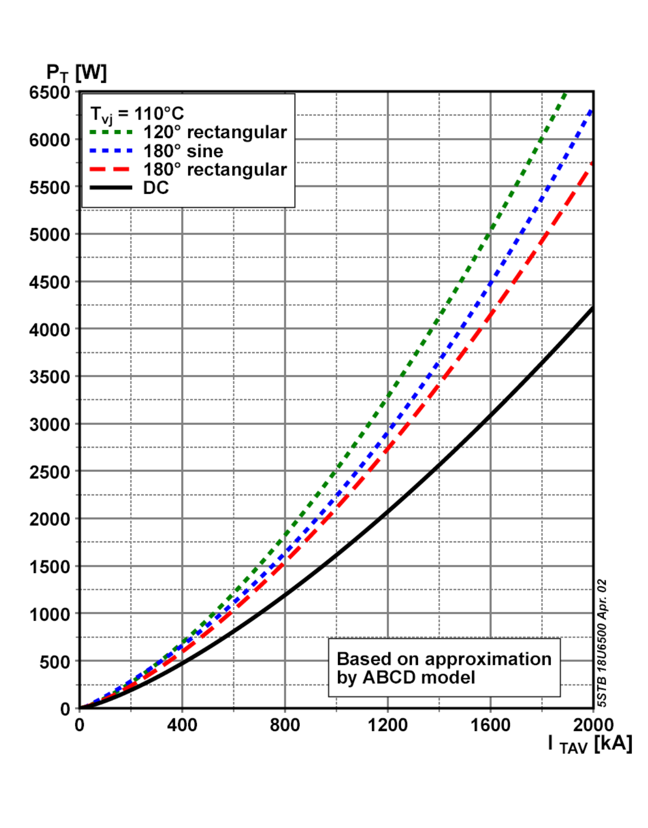

Fig. 4 On-state power dissipation vs. mean on-state current. Switching losses excluded.

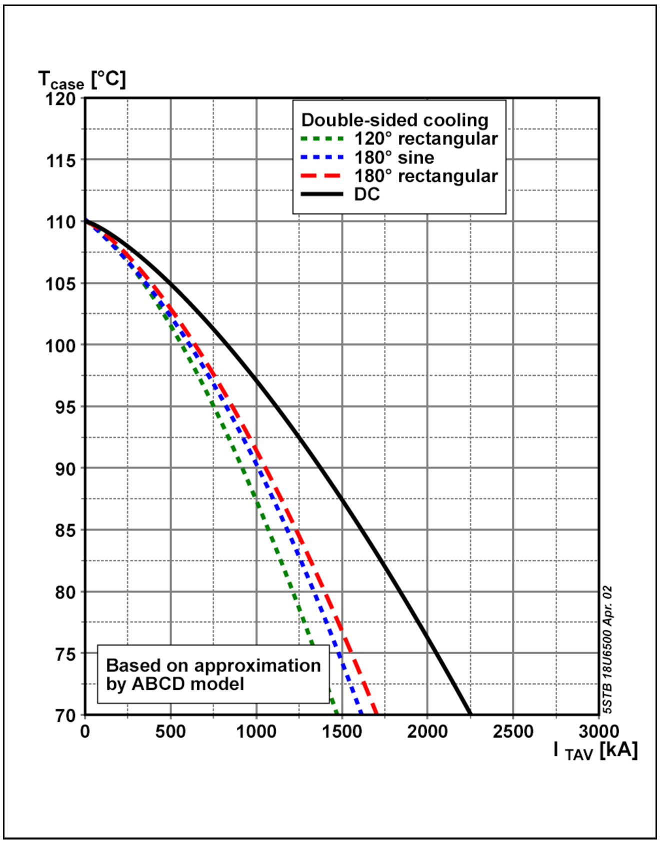

Fig. 5 Max. permissible case temperature vs. mean on-state current.

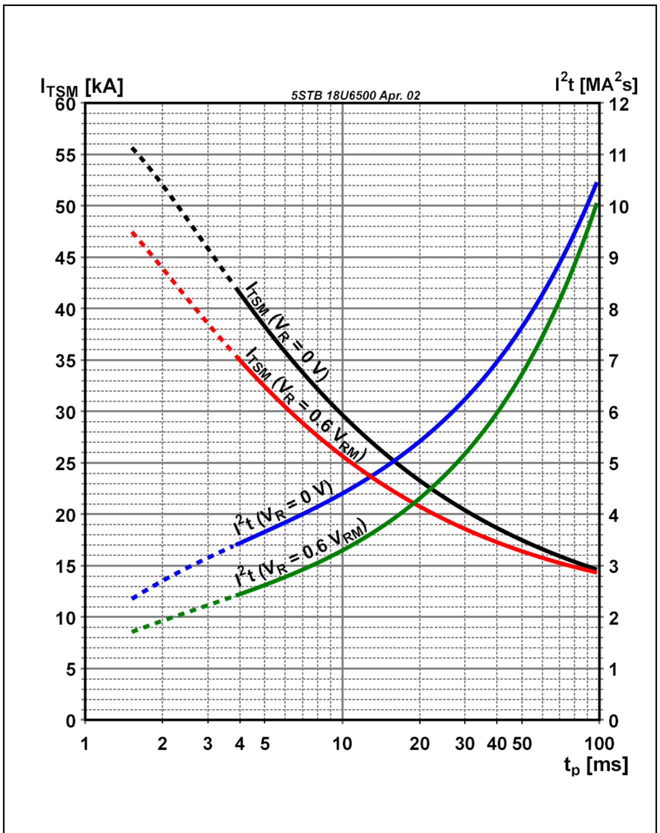

Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

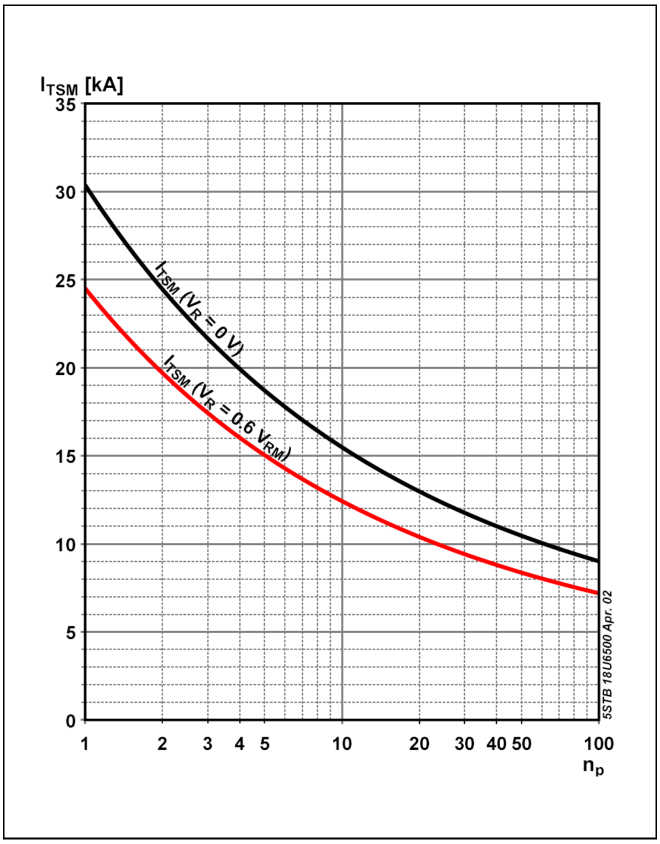

Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

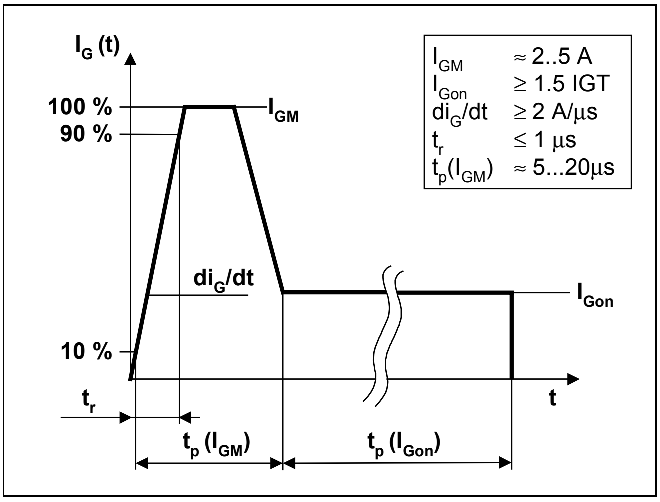

Fig. 8 Recommendet gate current waveform.

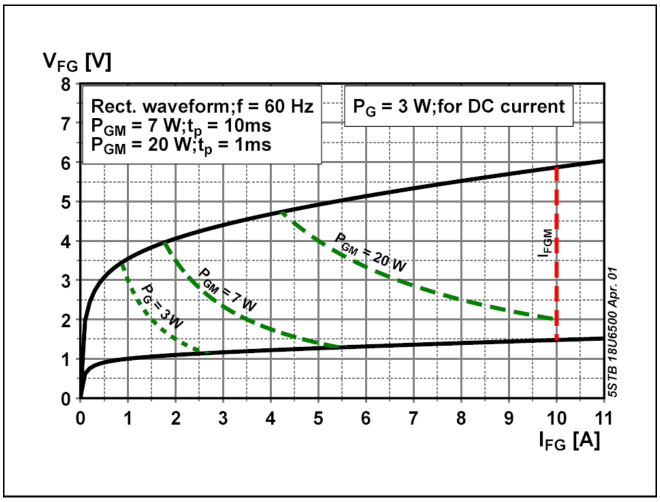

Fig. 9 Max. rated peak gate power loss.

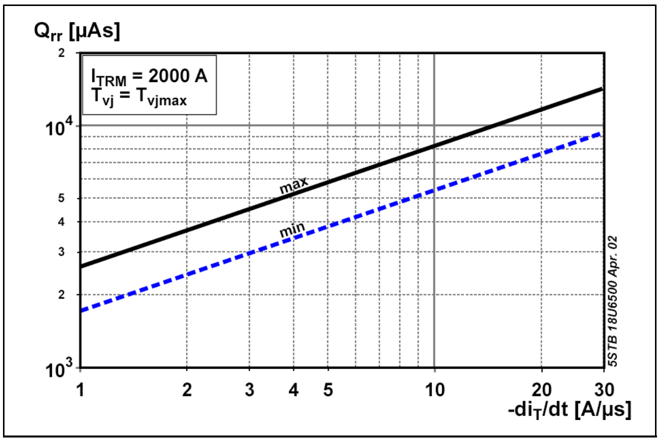

Fig. 10 Recovery charge vs. decay rate of on-state current.

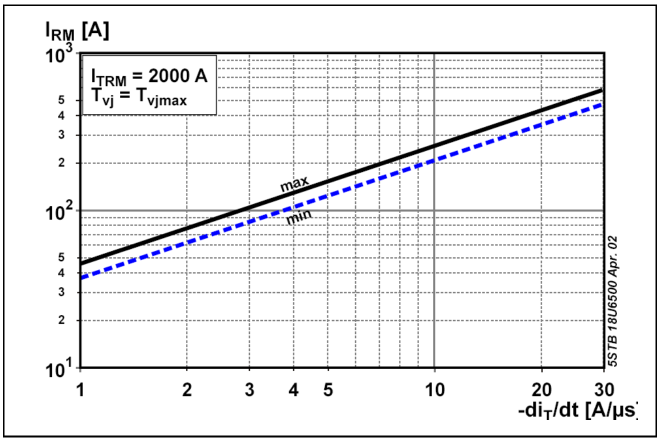

Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

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